In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Please substitute the following clean-text claim for claim 1.

1. (Currently Amended) [[An]] A computer ~~apparatus~~ comprising:

logic configured to analyze information relating to the network; and

logic configured to determine, based on the analyzed information, whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element ~~includes a~~ is a field effect transistor~~, wherein said logic is a computer configured to execute a rules checker program, wherein when the rules checker program is run on the computer, the rules checker program analyzes the information relating to the network to determine whether or not the element is a feedback element, wherein the element is a field effect transistor~~.

2. Canceled.

3. (Previously Presented) The apparatus of claim 1, wherein the rules checker program first determines whether or not the element being evaluated is a comprised in a recycle loop, wherein if a determination is made that the element is not comprised in a recycle loop, the rules checker program determines that the element is not a feedback element.

4. (Original) The apparatus of claim 3, wherein if the rules checker program determines that the transistor is comprised in a recycle loop, then the rules checker program determines whether or not a source or drain terminal of the transistor is connected to a RAM cell, wherein if the rules checker program determines that the source or drain of the

transistor is connected to a RAM cell, the rules checker program determines that the transistor is a feedback element.

5. (Original) The apparatus of claim 4, wherein if the rules checker program determines that source or drain of the transistor is not connected to a RAM cell, the rules checker program determines whether or not a gate terminal of the transistor being evaluated is a precharge node, wherein if the rules checker program determines that the gate terminal of the transistor is a precharge node, the rules checker program determines that the transistor is not a feedback element.

6. (Original) The apparatus of claim 5, wherein if the rules checker program determines that the gate terminal of the transistor is not a precharge node, the rules checker program determines whether or not the gate terminal of the transistor corresponds to a block input of the network comprising the transistor, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is a block input, the rules checker program determines that the transistor being evaluated is not a feedback element.

7. (Original) The apparatus of claim 6, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is not a block input, then the rules checker program determines whether or not an output of a return inverter comprised by the recycle loop is only driven by the return inverter, wherein if the rules checker program determines that the output of the return inverter is only driven by the return inverter, the rules checker program determines that the transistor being evaluated is not a feedback element.

8. (Original) The apparatus of claim 7, wherein if the rules checker determines that the output of the return inverter is not driven only by the return inverter, the rules checker program determines whether or not a gate terminal of the transistor being evaluated is driven by a pass transistor, wherein if the rules checker program determines that the gate

terminal of the transistor is driven by a pass transistor, the rules checker program determines that the transistor being evaluated is not a feedback element, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is not driven by a pass transistor, the rules checker program determines whether or not the gate terminal is channel-connected to another transistor which is not controlled either by a clock or by an output of the logic gate comprising the transistor being evaluated, wherein if the rules checker program determines that the gate terminal is not channel-connected to another transistor which not is controlled by a clock or by an output of the logic gate comprising the transistor being evaluated, the rules checker program determines that the transistor being evaluated is a feedback element.

9. (Original) The apparatus of claim 8, wherein the recycle loop comprises a first inverter and a second inverter, the transistor being evaluated being comprised in the first inverter, the first inverter corresponding to said logic gate, wherein if the rules checker program determines that the gate terminal is channel-connected to another transistor which is not controlled either by a clock or by an output of the logic gate comprising the transistor being evaluated, the rules checker program determines whether an N field effect transistor network and a P field effect transistor network comprised in the first inverter are both stronger than an N field effect transistor network and a P field effect transistor network, respectively, comprised in the second inverter, wherein if the rules checker program determines that the N field effect transistor network and the P field effect transistor network comprised in the first inverter are both stronger than the N field effect transistor network and the P field effect transistor network comprised in the second inverter, the rules checker program determines that the transistor being evaluated is not a feedback element.

10. (Original) The apparatus of claim 9, wherein if the rules checker program determines that the N field effect transistor network and the P field effect transistor network comprised in the first inverter are both stronger than the N field effect transistor network

and the P field effect transistor network comprised in the second inverter, the rules checker program determines whether an N field effect transistor network and a P field effect transistor network comprised in the first inverter are both weaker than the N field effect transistor network and the P field effect transistor network, respectively, comprised in the second inverter, wherein if the rules checker program determines that the N field effect transistor network and the P field effect transistor network comprised in the first inverter are not both weaker than the N field effect transistor network and the P field effect transistor network comprised in the second inverter, the rules checker program determines that the transistor being evaluated is a feedback element.

11. (Previously Presented) The apparatus of claim 1, wherein the rules checker program determines whether or not the transistor being evaluated is a feedback element by determining whether or not the transistor is comprised in a particular type of circuit, the particular type of circuit corresponding to a special case, wherein if the rules checker program determines that the element being evaluated is comprised in the particular type of circuit, the rules checker program determines that the transistor being evaluated is a feedback element.

12. (Original) The apparatus of claim 11, wherein the particular type of circuit corresponds to a zero catcher circuit and wherein the rules checker program performs a plurality of checks to determine whether or not the particular type of circuit is a zero catcher circuit.

13. (Original) The apparatus of claim 12, wherein the particular type of circuit corresponds to a ones catcher circuit and wherein the rules checker program performs a plurality of checks to determine whether or not the particular type of circuit is a ones catcher circuit.

14. (Currently Amended) A method comprising ~~the step of~~:

analyzing, by a computer, information relating to the network; and ~~to determine~~ determining, based on the analyzing, whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element is ~~includes~~ a field effect transistor~~, wherein the analyzing step is performed by a computer configured to perform the analysis, wherein said computer is configured to execute a rules checker program, wherein when the rules checker program runs on the computer, the rules checker program analyzes the information relating to the network to determine whether or not the element is a feedback element, wherein the element is a field effect transistor~~.

15. Canceled.

16. (Previously Presented) The method of claim 14, wherein during the analyzing step, the rules checker program first determines whether or not the element being evaluated is comprised in a recycle loop, wherein if a determination is made that the transistor is not comprised in a recycle loop, the rules checker program determines that the transistor is not a feedback element.

17. (Original) The method of claim 16, wherein if, during the analyzing step, the rules checker program determines that the transistor is comprised by a recycle loop, then the rules checker program determines whether or not a source or drain of the transistor is connected to a RAM cell, wherein if the rules checker program determines that the source or drain of the transistor is connected to a RAM cell, the rules checker program determines that the transistor is a feedback element.

18. (Original) The method of claim 17, wherein if, during the analyzing step, the rules checker program determines that the source or drain of the transistor is not part of a

RAM cell, then the rules checker program determines whether or not a gate terminal of the transistor being evaluated is a precharge node, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is a precharge node, the rules checker program determines that the transistor being evaluated is not a feedback element.

19. (Currently Amended) A computer program comprising:

a first code segment which analyzes information relating to ~~the~~ a network; and

a second code segment configured to determine, based on the analyzed information, whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element includes a transistor;[[,]]

wherein the first code segment first determines whether or not the element being evaluated is comprised in a recycle loop, wherein if a determination is made by the first code segment that the transistor is not comprised in a recycle loop, the program determines that the transistor is not a feedback element.

20. Canceled.

21. (Previously Presented) The program of claim 19, wherein if the first code segment determines that the transistor is comprised by a recycle loop, then the first code segment determines whether or not a source or drain of the transistor is connected to a RAM cell, wherein if the first code segment determines that the source or drain of the transistor is connected to a RAM cell, the program determines that the transistor is a feedback element, and wherein if first code segment determines that the source or drain of the transistor is not part of a RAM cell, then the first code segment determines whether or not the gate terminal of the transistor is a precharge node, wherein if the rules checker program determines that the gate terminal of the transistor is a precharge node, the rules checker program determines that the transistor is not a feedback element.

22. (Original) The computer program of claim 19, wherein the first code segment determines whether or not the element being evaluated is a feedback element by determining whether or not the element is comprised in a particular type of circuit, the particular type of circuit corresponding to a special case, wherein if the first code segment determines that the element being evaluated is comprised in the particular type of circuit, the first code segment determines that the element being evaluated is a feedback element.